Theoretical Efficiency for Triplers Using Nonideal Varistor Diodes at Submillimeter Wavelengths

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Abstract—**The theoretical efficiency for frequency triplers multiplying from 300 to 900 GHz has been calculated for nonideal GaAs Schottky diodes operating in the varistor mode. The maximum efficiency is determined to be about 7 percent, only slightly smaller than that for ideal varistors. Guidelines for optimum bias conditions and embedding network impedances have been determined using the large-signal analysis computer program of Siegel and Kerr [1].**

I. Introduction

THE CHOICE OF sources in the submillimeter wavelength regime is very restricted. Reliable fundamental sources with powers of tens of milliwatts exist for frequencies up to about 100 GHz in the form of Gunn oscillators, 200 GHz in the form of klystrons, and 400 GHz in the form of carcinotrons. Above 400 GHz, gas lasers—both unwieldy and difficult to use—provide the only fundamental sources. Multiplication of lower frequency fundamental sources presents an attractive alternative in this wavelength range.

In this paper, we seek to optimize the design and operation of the frequency multiplier most effective in submillimeter wavelength region: the GaAs Schottky-barrier diode multiplier operating in the varistor mode. The varistor mode represents one of two types of nonlinear diode impedance: the varactor with a nonlinear capacitance–voltage relationship and the varistor with a nonlinear current–voltage relationship. The harmonic generation efficiency of the varactor theoretically exceeds that for the varistor since a varactor suffers no resistive losses. However, in the wavelength range considered, currently available varistors are more efficient than varactors because they have considerably higher cutoff frequencies. In addition, the voltage range of variable capacitance in varactor diodes, a key factor in high-efficiency performance, decreases with increasing frequency.

Guidelines for optimizing varactor multipliers have long been established [2]. We present a similar analysis for frequency multiplication arising from the nonlinear resistance of the varistor multiplier. It has been shown that, for an ideal varistor (one with an infinitely high cutoff frequency), the conversion efficiency to the nth harmonic is the inverse of n^2 [3], [4]. Actual efficiency, however, is reduced due to losses in parasitic multiplier elements. Design guidelines seek to minimize this deviation from the ideal in physical multipliers.

To establish such design guidelines, we examine the dependence of multiplier performance on its operating point, embedding network (i.e., diode mount), and diode parameters. Dependence is established empirically by methodically sampling parameter configurations and the frequency conversion efficiencies they yield. Efficiency sensitivity to individual design parameters, and the optimum values for these parameters, is then determined from the sampled points.

Such sampling requires an analytic tool capable of determining multiplier performance from the relevant design parameters. The tool employed here evolved from the large-signal analysis subroutine of the mixer analysis program (GISSMIX) by Siegel and Kerr [1], later modified by Siegel, Kerr, and Hwang [5] for multiplier analysis. This program simulates the behavior of the diode as it settles to a steady-state response, iterating through time the diode state equations as it interacts with its embedding network. Through repeated execution of the program at varied design parameter configurations, the efficiency-parameter sampling required to establish design guidelines can be performed.

We apply this technique to study a tripler, with input frequency at 300 GHz and output frequency at 900 GHz. The diode parameters used are characteristic of state-of-the-art GaAs Schottky-barrier mixer diodes [6]. Such a multiplier could employ a carcinotron as its pump source and be implemented with a combination of waveguide and quasi-optical components.

II. Analytic Method

A. The Multiplier Analysis Problem

Frequency multiplication in a varistor diode derives from the same principle as that of its counterpart, the varactor diode. Both regimes of diode performance are characterized by nonlinear impedance transfer functions, converting an input sinusoidal waveform into a distorted waveform with harmonics present. Both types of imped-

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ance nonlinearity, capacitive and resistive, are incorporated in the two equations of state governing diode behavior over its entire operational range.

The total current in the diode I_d arises as a superposition of two generated currents. The first current component I_g stems from the conductance effects of the diode junction, as given by thermionic emission theory

$$I_g = I_s[e^{\alpha V_d} - 1]$$

where $\alpha = q/\eta kT$, η is the diode ideality factor (1 being ideal), and I_g is the diode saturation current.

The second current component I_c arises from the junction's capacitive effects. The junction capacitance C, inversely related to the depletion-layer thickness, and hence the reverse voltage, is given by

$$C = C_0[1 - V_d/\phi]^{-\gamma}$$

where C_0 is the junction capacitance at $V_d = 0$, ϕ is the diode contact potential, and γ is dependent on the change distribution within the depletion layer. This capacitive effect dominates the performance of the ideal varactor diode, assumed to exhibit negligible conductance; conversely, it is assumed negligible for the ideal varistor diode, driven primarily by conductance effects.

Mediating the diode's response are its own series resistance and the impedance of its mount, represented as an embedding network in the frequency domain. The series resistance R_s arises from the diode material itself, depending both on diode geometry and on frequency, as approximated by the skin effect. The generalized embedding network has known (measured) impedance Z_e, n at each harmonic n of the input frequency. Biases are applied to this network at dc and the pump frequency, determining by Kirchoff's laws boundary conditions at the diode.

This boundary-value problem cannot generally be solved in closed form; iterative methods of solution must be employed. To facilitate such iterative solution, Kerr introduced an additional hypothetical element into the equivalent circuit model [7]. He modeled the diode junction–network interface as a lossless transmission line of characteristic impedance Z_0. With the transmission-line length set to an integral number of pump wavelengths, the steady-state harmonic waveforms remain unaffected by this artifice. Where the traditional model posed a dynamic boundary condition, Kerr's approach poses an unbalanced system whose settling behavior is well-defined. A schematic drawing of the embedding network, connecting transmission line, and diode model is shown in Fig. 1. An initial right-propagating wave induces in the diode junction a left-propagating wave, which traverses the transmission line and is reflected at the embedding network to produce a new right-propagating wave. This reflection cycle is repeated in a progression that can be analytically simulated through time. When both waves become equal in magnitude, a steady-state solution is attained. An explicit discussion of this technique can be found in Siegel, Kerr, and Hwang [5].

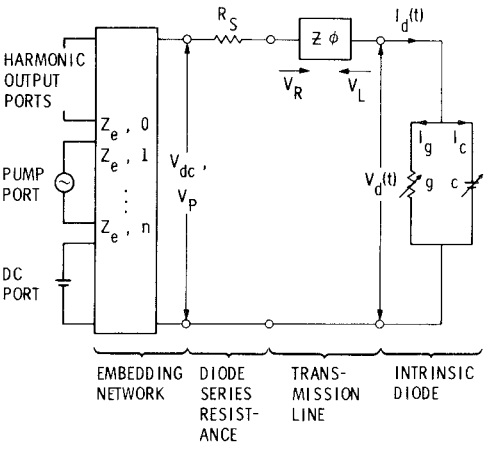

Fig. 1. The embedding network, connecting transmission line, and diode model used for the computer simulation.

B. Program Implementation

Our program implementation closely parallels that of Siegel and Kerr [1] for the analysis of mixers. However, because multipliers are optimized differently than mixers, we have altered the operating point variables in the GISSMIX program. Rather than adjusting a local oscillator power until a desired rectified current flows, frequency multipliers are usually set to a fixed pump power level while the dc bias voltage or current level is varied to obtain optimum efficiency. Therefore, we take the pump power and not the dc bias current to be the independent variable for the multiplier. We have modified the program to reflect these needs. (Siegel, Kerr, and Hwang [5] have carried out similar modifications; however, their implementation—in particular, their method of calculating powers—differs slightly from ours.) In addition, we have restructured the logic flow in the large-signal analysis program to facilitate understanding and ease of modification.

Given three sets of input parameters—describing the diode, its embedding network, and its operating point—the computer program iterates the reflection cycle analysis above until it converges to the desired operating point. It then computes the diode steady-state performance parameters. The relevant diode input parameters are: series resistance R_s(dc), coefficient R_{skin} for the skin effect, saturation current I_s, zero bias junction capacitance C_0, contact potential ϕ, charge distribution descriptor γ, and ideality factor η. These parameters fully describe the diode response to an incident voltage signal, as detailed by the current equations and shown in Fig. 1. The input embedding network parameters are: the number of harmonics considered and the complex impedances $(R_s(nf_p) + jX_e(nf_p))$ at each.

Having thus determined the elements of the multiplier equivalent circuit, the system's description is completed by setting its operating point parameters: pump frequency, operating temperature, bias current for varistors (or voltage for varactors), and pump power. These operating point parameters sufficiently characterize the multiplier's performance; however, they do complicate the analysis. Their

selection precludes direct application of the initial boundary value problem analysis of Section II-A because the operating point parameters themselves comprise a partial description of the diode's steady-state behavior, and not a statement of initial diode voltages.

The driven voltage signals V_{dc} and V_p at the diode corresponding to the desired operating point are set initially to their optimal values from a power efficiency standpoint: the embedding impedance is calculated assuming conjugate matching between the embedding network and the physical diode (including series resistance) to maximize the power delivered at the diode.

With these initial values established, the program enters the power adjustment computation loop, designed to adjust the V_p estimate until the Kerr reflection cycle analysis yields the desired steady-state pump power absorbed in the physical diode. The program remains in this loop until both the pump power and steady-state convergence (tested by an embedding network/diode current comparison) are achieved within a set accuracy, or until a set maximal number of adjustments have been made.

Nested in the power adjustment loop is the core of the simulation, the reflection cycle analysis loop. For the preset value of V_p, this loop first solves the diode state equations to yield the left-traveling waveform triggered by the incident voltage. The new diode voltage and current waveforms are then transformed to the frequency domain. A ratio of the diode/mount current flow is computed for convergence checks, and new left- and right-traveling voltages are determined using the transmission-line model of Section II-A. At this point in the power adjustment loop, the pump power absorbed by the physical diode at this multiplier operating point is assessed and compared to the input power and V_p is adjusted accordingly to approach the desired input power.

While we retain the capacity to use the power available from the source, a variable more easily determined in the laboratory, as the input parameter, we use the absorbed power as our variable operating point for several reasons. We employ the program for design use, and the actual power absorbed at the diode provides a more direct measure of the optimal diode operating point. When power available is used as the input parameter, the power absorbed in the diode is dependent on both the operating point and the embedding network impedance at the pump frequency and thus is not a constant of the optimizing procedure. The optimum efficiency occurs when the mount is designed with an impedance conjugately matching that of the physical diode. We assume such a case possible in the optimum design, and provide as an output parameter the calculated embedding impedance at the pump frequency. For other uses of the program, such as predicting the laboratory performance of an existing multiplier, power available is the relevant parameter.

When the voltage is sufficiently well guessed to give a steady-state solution with the desired pump power, the program proceeds to the final computation of the steady-state parameters. The output parameters include the conductance and capacitance Fourier coefficients, the voltage and current Fourier coefficients, the conversion efficiency at each harmonic, the diode impedance at each harmonic, and the maximum voltage swing.

C. Program Verification

We have verified the accuracy of the large-signal analysis part of the GISSMIX program, modified as described above, by comparing its results to those for varactor diode doublers and triplers derived by Penfield and Rafuse [2]. Our testing scheme for such multipliers has two goals: first, a concise check of the program's validity over the entire frequency range, and second, a thorough check of all computed parameters for selected cases. For the test cases, then, computed efficiencies, diode current and voltage waveforms, and pump impedances were checked against closed-form predictions of Penfield and Rafuse.

The varactor model consists of two elements, a nonlinear capacitance and a constant series resistance. The nonlinear capacitance of the abrupt-junction varactor varies with diode voltage as given in Section II-A, with $\gamma = 0.5$. It is assumed that the forward voltage never exceeds the contact potential ϕ (when $v = \phi$, the capacitance becomes infinitely large) and that the reverse voltage never exceeds the breakdown voltage. Further, for these ideal varactors, no dc current flows; the saturation current is assumed to be 0. Values for the impedances at the input and output frequencies are determined by Penfield and Rafuse's criteria for maximum conversion efficiency. The mount is terminated in an open circuit for the higher harmonics, with tuned and lossless idlers. For the purposes of testing the program, we have used the diode parameters given in Table I. The same parameters are used in all test cases and not meant to represent any real diode.

Applying this testing scheme to the doublers and triplers gives excellent results as shown in Table II. For the doubler, the efficiencies computed obey optimal theoretical predictions throughout the frequency range, with pump frequencies of 5 to 5000 GHz. For five test cases, we obtain a standard deviation of 1.4 percent from the theoretical efficiency, with the maximum deviation in any one case being 2.2 percent. The diode waveform coefficients for the voltage, current, and pump impedance also show excellent agreement with theory. The standard deviations are all within 3 percent, and generally within 1 percent, with the maximum deviation being 4.1 percent.

The tripler results also show good agreement with theory. We tested cases from 5 to 500 GHz. For the four test cases, we obtain a standard deviation of 6 percent from the maximum efficiency, and standard deviations of under 5 percent for all the harmonic waveforms. The worst cases have deviations generally on the order of 6 percent with maximum deviations for the efficiency and third-harmonic waveforms of roughly 10 percent, all occurring for one run that was allowed to converge at 8 percent above the theoretical operating point in order to speed the analysis.

TABLE I
VARACTOR DIODE PARAMETERS USED FOR VERIFICATION OF PROGRAM

$f_c = 5000$ GHz
$R_s = 4.244\ \Omega$
$R_{skin} = 0.\ \Omega$
$I_s = 0.$ A
$C_0 = 15$ fF
$\phi = 0.5$ V
$\gamma = 0.5$
$\eta = 1.0$
$V_b = 1.5$ V

TABLE II
PROGRAM VERIFICATION RESULTS—STANDARD AND MAXIMUM DEVIATION OF COMPUTED PARAMETERS FROM THE PENFIELD AND RAFUSE CALCULATIONS.

	Standard Deviation	Maximum Deviation
A. The doubler		
efficiency	1.4%	2.2%
V_1	0.4%	0.6%
V_2	1.8%	2.7%
I_1	0.4%	0.7%
I_2	2.6%	4.1%
R_1	0.9%	2.1%
X_1	0.2%	0.3%
B. The tripler		
efficiency	6.0%	9.6%
V_1	1.9%	4.4%
V_2	1.7%	3.8%
V_3	4.2%	9.8%
I_1	3.2%	6.8%
I_2	3.4%	6.2%
I_3	4.9%	10.1%
R_1	4.1%	6.0%
X_1	1.6%	2.7%

III. THE VARISTOR DIODE TRIPLER

We have used the modified GISSMIX program to determine the design parameters for a frequency tripler with input frequency at 300 GHz and output frequency at 900 GHz. Since varactor diodes are inefficient in the submillimeter-wave regime, the nonlinear element is chosen to act as a varistor, with no voltage-dependent capacitance. Following Penfield and Rafuse, we use an idler frequency at 2 f_p.

A. Diode Parameters and Bias Conditions

The diode parameters used as input to the tripler runs are summarized in Table III. These parameters were chosen to represent the state-of-the-art in high-frequency mixer diodes and to suppress the voltage dependence of the capacitance so that the results could be assessed solely in terms of varistor-mode operation.

The series resistance, chosen to be 10 Ω, is slightly higher than that typically measured at dc. However, this resistance is increased in the submillimeter regime by the skin effect that contributes about 3 to 5 Ω in the frequency range we are considering. The skin resistance was set at 0 Ω to simplify the analysis and interpretation of the results and to make it more comparable to the Penfield and Rafuse formulation. The saturation current is usually determined by extrapolating the log of the dc $I-V$ curve for a GaAs diode. This extrapolation depends somewhat on the data points taken, but is typically about $0.5–1.0\times10^{-16}$ A [8]. The zero-bias junction capacitance was taken to be 1 fF because this is the lowest capacitance device made by Mattauch at the University of Virginia [6]. In these calculations, the variation of capacitance with voltage was suppressed by setting γ to 0. For that reason, the value for ϕ, the built-in potential, is immaterial. Although most diodes do have a variable capacitance resulting in a varactor contribution, this is minimal for Mott diodes used for mixer applications. Further, at the high submillimeter frequencies considered here, the voltage range over which the capacitance varies is reduced. The ideality factor η was set to 1.2 because, again, that is representative of diodes operated at room temperature, obtained from Mattauch at the University of Virginia.

TABLE III
VARISTOR DIODE PARAMETERS USED IN TRIPLER CALCULATIONS

R_s	10 Ω
R_{skin}	0 Ω
I_s	1.0×10^{-16} A
C_0	1.0 fF
f	1.0 V
g	0.0
h	1.2

The bias parameters were systematically varied over a given range. The pump power was set at two levels, 4 mW and 40 mW. The higher value was chosen since it is typical of the power obtained from a carcinotron at 300 GHz. The lower value was chosen because there may be substantial loss in coupling that power into the multiplier. The dc bias current was varied in the range 3–25 mA. This range was dictated by the optimum results. An operating temperature of 300 K was assumed.

B. The Embedding Network Impedances

The optimum impedances at dc and the pump frequencies are determined by the program. At dc, the independent parameter is the diode current. The mount impedance can be set at any convenient value, in this case 200 Ω, following Siegel and Kerr [4]. At the pump frequency, the program calculates the embedding network impedance so that the specified pump power is absorbed completely in the physical diode. This impedance actually becomes an output of the program rather than an input. It also implies that each run represents a different physical realization of the embedding network. This differs significantly from previous applications of this program where the mount impedance is set to represent a given device. We follow this procedure since our goal is to determine the optimum impedances, rather than verify how well a given mount realization performs. The real part of the impedance at the idler frequency $2f_p$ is set to zero to minimize loss. The imaginary part is set to resonate out the junction capacitance at that frequency. This tuned impedance may not

TABLE IV
RESULTS WITH THIRD-HARMONIC REACTANCE OPTIMIZED FOR A GIVEN PUMP POWER, DC BIAS, AND THIRD-HARMONIC RESISTANCE

I_{dc}	$X_e(3f_p)$	$R_d(f_p)$	$X_d(f_p)$	V_d	V_b	Eff(1 → 3)
Power = 4 mW, $R_e(3f_p) = 30\ \Omega$						
3	120	306.5	−258.7	−0.14	−4.04	6.03%
5	90	191.4	−38.9	0.41	−2.22	6.17%
7	70	108.5	−5.0	0.66	−1.38	5.88%
Power = 4 mW, $R_e(3f_p) = 50\ \Omega$						
3	120	278.6	−255.8	−0.13	−3.76	6.06%
5	90	183.7	−55.2	0.39	−2.11	6.33%
7	70	106.2	−14.5	0.65	−1.27	6.02%
10	40	54.2	−3.9	0.90	−0.46	4.95%
Power = 4 mW, $R_e(3f_p) = 100\ \Omega$						
3	120	248.4	−249.8	−0.14	−3.53	4.84%
5	90	171.3	−74.0	0.38	−2.00	5.34%
10	40	54.8	−9.4	0.89	−0.50	4.10%
Power = 40 mW, $R_e(3f_p) = 30\ \Omega$						
3	170	89.3	−514.1	−8.86	−33.08	2.51%
5	150	174.2	−476.4	−5.49	−23.91	4.79%
7	140	255.0	−395.9	−3.73	−18.91	5.60%
10	120	304.5	−225.2	−2.29	−14.37	6.43%
15	90	209.6	−48.9	−0.97	−9.75	6.77%
20	70	124.3	−8.0	−0.19	−6.96	6.62%
Power = 40 mW, $R_e(3f_p) = 50\ \Omega$						
10	120	276.4	−255.0	−2.27	−13.48	6.47%
15	90	192.9	−63.3	−0.92	−9.01	6.85%
20	80	126.1	−21.9	−0.25	−6.99	6.77%
Power = 40 mW, $R_e(3f_p) = 100\ \Omega$						
10	120	244.1	−231.3	−2.36	−12.93	5.22%
15	90	178.5	−83.5	−0.98	−8.65	5.76%
20	70	119.3	−36.7	−0.28	−6.53	5.71%
25	60	81.6	−18.5	0.24	−5.03	5.34%

yield the highest efficiency and could be studied further. The impedance at the third harmonic, the output frequency, is systematically varied. The real part of the impedance was set to 30, 50, and 100 Ω. This range encompasses the impedance of most antenna structures. The imaginary part was varied, in 10-Ω steps, over a range dictated by the location of the optimum harmonic conversion efficiency. The impedances at higher harmonics were set to an open circuit. A short circuit would probably yield improved performance; however, an open circuit or high impedance is easier to realize at the frequencies involved.

C. The Results

The output of the program for the runs corresponding to the optimum value of imaginary impedance at the third harmonic are summarized in Table IV. The maximum tripler efficiency is determined to be about 7 percent, slightly smaller than the 11 percent expected for the ideal

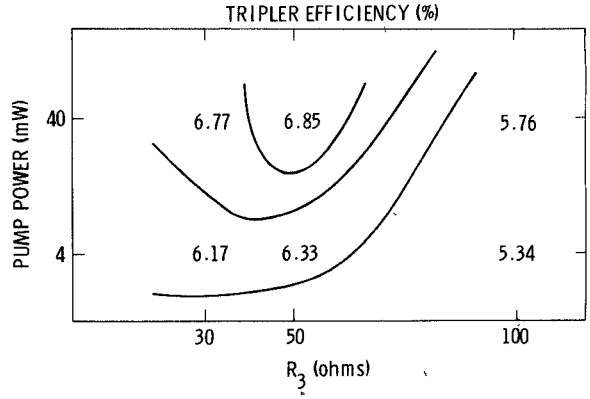

Fig. 2. Contour plot of the computed tripler efficiency for the varistor diode as a function of the pump power and the real part of the third-harmonic impedance.

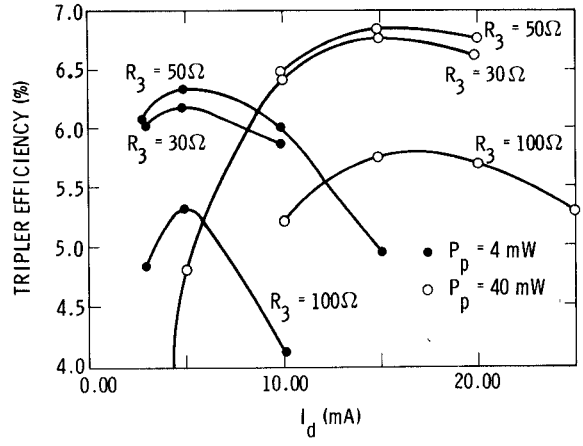

Fig. 3. The tripler efficiency as a function of dc drive current parameterized by the pump power and real part of the embedding network impedance at the third harmonic.

varistor. A contour plot of the optimal conversion efficiency for three different mount structures as a function of pump power and $R_e(3f_p)$ is shown in Fig. 2. For the range of these parameters tested, the maximum efficiency occurs at $R_e(3f_p) = 50\ \Omega$ and pump power = 40 mW. In the following, we present the sensitivity of the conversion efficiency to the bias conditions and embedding network impedances.

The efficiency as a function of diode current I_d parameterized by pump power and the real part of the impedance at the third harmonic is shown in Fig. 3. The efficiencies shown have been maximized with respect to the imaginary part of the impedance at the third harmonic. The current at which maximum efficiency occurs depends on the pump power but not on the mount impedance. For a pump power of 4 mW, the current is about 5 mA, whereas for a pump power of 40 mW, that current is about 15 mA. In practice, currently available state-of-the-art GaAs mixer diodes burn out if operated at more than about 10-mA drive current for extended periods of time. Therefore, it may be impractical to pump such a diode with 40 mW of power.

V_{dc}, the voltage at the physical diode, for the various runs is given in Table IV. As for the diode current, the

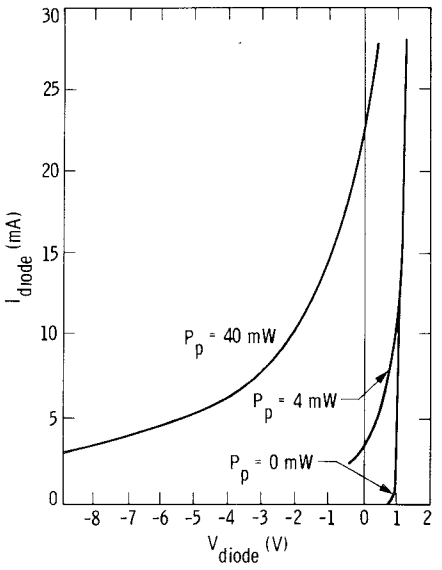

Fig. 4. The dc $I-V$ curve for the diode pumped with 0, 4, and 40 mW of power at 300 GHz.

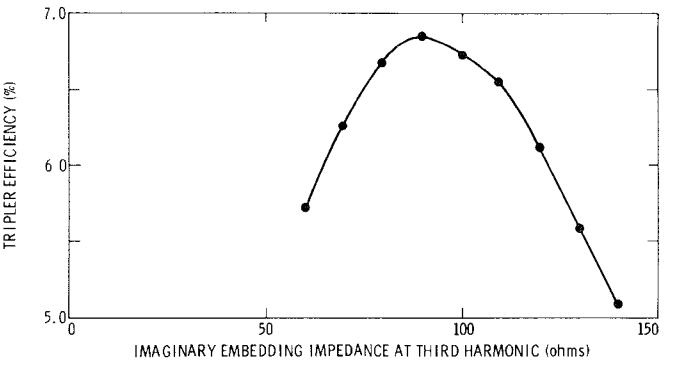

Fig. 5. The dependence of the tripler efficiency as a function of third-harmonic imaginary impedance for a drive power of 4 mW, a dc-bias current of 5 mA, and a third-harmonic real impedance of 50 Ω.

optimum value depends on pump power but not the embedding network impedance. For a pump power of 4 mW, it is about 0.4 V, while for 40 mW it is about −0.9 V. Note that even though the diode is operating solely in the varistor mode (the voltage dependence of the capacitance is suppressed), it requires reverse bias for optimum operation if it is pumped with large powers. This can be understood from Fig. 4, where the $I-V$ characteristic of the diode is shown for 0, 4, and 40 mW of drive power. The pumped diode draws positive current for reverse biases.

Another design parameter for diodes is the reverse breakdown voltage V_b. An output of the program is the instantaneous maximum value of the voltage swing in the diode. The reverse breakdown voltage must be greater than the largest instantaneous reverse voltage experienced by the diode. These voltages are summarized in Table IV. In general, the required breakdown voltage is a function of both pump power and dc bias. It is larger for high pump powers since they determine the peak to peak voltage swing. Further, the dc bias point determines the average value, so the breakdown voltage increases as the diode current decreases. For the diode parameters tested here, the required V_b is about −2 V when driven by 4 mW, and about −9 V when driven by 40 mW. It is interesting to note that in some cases where both the efficiency and current are quite low, the required breakdown voltage can be quite large. For instance, when $I_d = 3$ mA, $P_p = 40$ mW, and $R_e(3f_p) = 30$ Ω, the required $V_b = -33$ V. This phenomenon could explain some mysterious failures of diodes. We should point out that the breakdown voltages presented here are for optimum tuning only and do not indicate the maximum safe V_b for a given mount under all operating conditions.

As can be seen in Table IV or Fig. 2, the efficiency is largest when the real part of the mount impedance is about 50 Ω for a fixed bias condition. The efficiency at 30 Ω is not significantly lower than that at 50 Ω, whereas that at 100 Ω is reduced by about 20 percent. The sensitivity of tripler efficiency to the imaginary part of the impedance at the output frequency is much more dramatic, as can be seen in Fig. 5. The optimum conversion efficiency was obtained when $Xe(3f_p)$ was about 90 Ω, independent of the real part of the impedance. This is considerably lower than the impedance required to tune out the zero-bias capacitance at the third harmonic, about 177 Ω. A consequence of this is that the current and voltage waveforms were not in phase at the third harmonic. The relationship between the third-harmonic conversion efficiency and the total diode current at the third harmonic is virtually linear. This is illustrated in Fig. 7 where these two variables are plotted as a function of each other for all the runs for which the pump power is 40 mW and $R_e(3f_p)$ is 30 Ω. While the cause of this effect is not known, the diode waveforms demonstrate dependence on $X_e(3f_p)$ consistent with this efficiency curve. For instance, the diode current at the third harmonic demonstrates a bell-shaped curve peaking at 90 Ω. More detailed examination of our results show that this maximum in both current and efficiency occurs when the capacitive and conductive contributions to the diode current are equal in magnitude and most in phase, regardless of either current's phase relation to the voltage. This result suggests that the maximizing output current is more relevant than tuning output current and voltage in maximizing efficiency.

At the idler frequency $2f_p$, the real part of the impedance has been set to 0 while the imaginary part was set to 265 Ω, the value required to tune out the 1-fF junction capacitance of the diode. The magnitude of the current and voltage Fourier components at this frequency are about the same as the magnitude of current and voltage at the third harmonic. No power is generated at this frequency, however, since the current and voltage waveforms are 90 degrees out of phase. We have not determined the sensitivity of the tripler efficiency to these impedances and suggest that they are not necessarily optimized.

The impedance at the pump frequency is determined by the program so that all the pump power is absorbed in the physical diode. This output from the program is given in

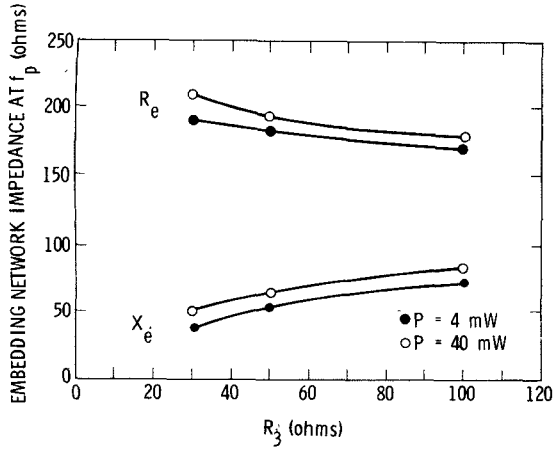

Fig. 6. The real and imaginary embedding network impedances at the pump frequency as a function of the real part of the embedding network impedance at the third harmonic parameterized by pump power for all the other parameters optimized.

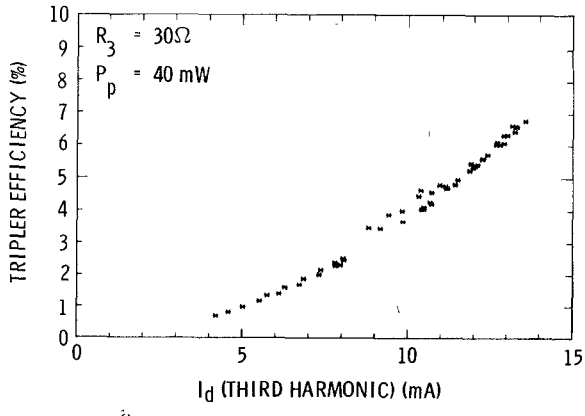

Fig. 7. The third-harmonic conversion efficiency for the varistor diode as a function of the magnitude of the current at the third harmonic for a 300-GHz pump power of 40 mW, and the real part of the embedding network impedance = 30 Ω.

Table IV as R_d and X_d. The mount impedance would be the complex conjugate of the diode impedance. The real and imaginary parts of the pump embedding impedance as a function of the real part of the mount impedance at $3f_p$ is shown in Fig. 6 for the optimum efficiency points. The best value for this impedance is approximately 190+j60 Ω. In the Penfield and Rafuse varactor analysis, this impedance is strongly a function of the ratio of pump frequency to cutoff frequency, a parameter we did not test.

The impedance at the higher harmonics has been set to 10M+j10M to simulate an open-circuit condition. Under these conditions, the amplitude of the voltage and current waveforms is very small. Application of this program to mixers (Siegel and Kerr) indicate that better performance is obtained when the higher harmonics are shorted out; however, measurements agree better with the computed results when they are open. In the submillimeter regime, a broad-band high-impedance termination is easier to achieve than a broad-band short circuit consistent with these observations.

D. Comparison to Laboratory Tripler Performance

A tripler to 900 GHz has not been demonstrated in the laboratory. Frequency doublers, where no idler circuit is required, operating as high as 700 GHz have been reported [9]. Frequency triplers to 450 GHz that produce 0.5 mW of output power with an efficiency of 2 percent (10), to 350 GHz that produce 1–3 mW of output power with an efficiency of about 1–3 percent [11], [12], and to 280 GHz that yield about 5-mW output power with a 6–8 percent efficiency [12], [13] have been reported. None of these submillimeter triplers have efficiencies exceeding the theoretical varistor limit of 11 percent. These devices for the most part employ varactor diodes; however, in the few cases where bias conditions are given, they operate at about 5-V reverse bias with from 0.5- to 10-mA forward current [11], [12] more indicative of varistor operation. Millimeter-wave doublers using varactor diodes have yielded efficiencies as high as 40 percent at 115 GHz [5], higher than the maximum doubling efficiency for varistors (25 percent), indicating that these devices must be operating in the varactor rather than the varistor mode.

Most of the above triplers have utilized waveguide, stripline, or coaxial structures for circuit implementation. These types of circuit elements require components that are on the order of the operating wavelength in size. For the submillimeter regime, they become more difficult to fabricate with the precision and accuracy necessary to yield good performance. Archer [12] has incorporated quasi-optical tuning elements for the idler and output circuits of a tripler that operates at 350 GHz. Frerking, Pickett, and Farhoomand [14] employed a quasi-optical diplexer for a doubler to 600 GHz. Similar techniques can be employed throughout the submillimeter band.

IV. Summary

We have carried out a theoretical evaluation of the GaAs Schottky diode tripler operating in the varistor mode. We find that the optimum tripler conversion efficiency from 300 to 900 GHz for a state-of-the-art diode is about 7 percent, only slightly smaller than that for the ideal varistor diode. The large-signal analysis subroutine of the program GISSMIX [1], modified for our application, was employed to establish design guidelines. The program was verified against the Penfield and Rafuse [2] results for varactor diodes. Optimum embedding network impedances at the pump and output frequencies were determined, as well as the dc bias conditions. Constraints on the reverse bias breakdown voltage were discussed.

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